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IEEE PROJECT TITLE 2017-18

DOMAIN : VLSI

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S.No	LOW POWER PROJECT TITES	DOMAIN
VLP01	A 2.5-ps Bin Size and 6.7-ps Resolution FPGA Time-to-Digital Converter Based on Delay Wrapping and Averaging	IEEE 2017-18 VLSI TITLES
VLP02	Coordinate Rotation-Based Low Complexity K-Means Clustering Architecture	
VLP03	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding	
VLP04	A Way-Filtering-Based Dynamic Logical–Associative Cache Architecture for Low-Energy Consumption	
VLP05	Resource-Efficient SRAM-based Ternary Content Addressable Memory	
VLP06	Write-Amount-Aware Management Policies for STT-RAM Caches	
VLP07	Fault Diagnosis Schemes for Low-Energy Block Cipher Midori Benchmarked on FPGA	
VLP08	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	
VLP09	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	
VLP10	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	
VLP11	Stochastic Implementation and Analysis of Dynamical Systems Similar to the Logistic Map	
VLP12	Efficient Designs of Multi-ported Memory on FPGA	
VLP13	High-Speed and Low-Latency ECC Processor Implementation Over GF(2m) on FPGA	
VLP14	An On-Chip Monitoring Circuit for Signal-Integrity Analysis of 8-Gb/s Chip-to-Chip Interfaces With Source-Synchronous Clock	
VLP15	A 2.4–3.6-GHz Wideband Sub-harmonically Injection-Locked PLL with Adaptive Injection Timing Alignment Technique	
VLP16	Hardware-Efficient Built-In Redundancy Analysis for Memory With Various Spares	
VLP17	Fast Automatic Frequency Calibrator Using an Adaptive Frequency Search Algorithm	
VLP18	A High-Efficiency 6.78-MHz Full Active Rectifier with Adaptive Time Delay Control for Wireless Power Transmission	
VLP19	Scalable Device Array for Statistical Characterization of BTI-Related Parameters	
S.No	**AREA EFFICIENT/ TIMING & DELAY REDUCTION PROJECT TITES**	
VAE01	VLSI Design of 64bit × 64bit High Performance Multiplier with Redundant Binary Encoding	
VAE02	ENFIRE: A Spatio-Temporal Fine-Grained Reconfigurable Hardware	

VAE03	Hybrid Hardware/Software Floating-Point Implementations for Optimized Area and Throughput Tradeoffs	**DOMAIN**
VAE04	Efficient Soft Cancelation Decoder Architectures for Polar Codes	**IEEE 2017-18 VLSI TITLES**
VAE05	Low-Complexity Digit-Serial Multiplier Over GF(2m) Based on Efficient Toeplitz Block Toeplitz Matrix–Vector Product Decomposition	
VAE06	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	
VAE07	FPGA Realization of Low Register Systolic All-One-Polynomial Multipliers over GF (2m) and Their Applications in Trinomial Multipliers	
VAE08	Low-Complexity Transformed Encoder Architectures for Quasi-Cyclic Non-binary LDPC Codes Over Subfields	
VAE09	Antiwear Leveling Design for SSDs With Hybrid ECC Capability	
VAE10	Energy-Efficient VLSI Realization of Binary64 Division with Redundant Number Systems	
S.No	**AUDIO, IMAGE AND VIDEO PROCESSING PROJECT TITES**	
VAIVP01	A Dual-Clock VLSI Design of H.265 Sample Adaptive Offset Estimation for 8k Ultra-HD TV Encoding	
VAIVP02	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	
VAIVP03	Energy-Efficient Reduce-and-Rank Using Input-Adaptive Approximations	
VAIVP04	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers	
VAIVP05	An FPGA-Based Hardware Accelerator for Traffic Sign Detection	
VAIVP06	Soft Error Rate Reduction of Combinational Circuits Using Gate Sizing in the Presence of Process Variations	
VAIVP07	Time-Encoded Values for Highly Efficient Stochastic Circuits	
VAIVP08	Design of Power and Area Efficient Approximate Multipliers	
S.No	**VERIFICATION PROJECT TITES**	
VVF01	COMEDI: Combinatorial Election of Diagnostic Vectors From Detection Test Sets for Logic Circuits	
VVF02	Reordering Tests for Efficient Fail Data Collection and Tester Time Reduction	
S.No	**VLSI - BACK END PROJECT PROJECT TITES**	
VBEP01	Temporarily Fine-Grained Sleep Technique for Near- and Sub-threshold Parallel Architectures	
VBEP02	Low-Power Design for a Digit-Serial Polynomial Basis Finite Field Multiplier Using Factoring Technique	
VBEP03	10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage	

VBEP04	Delay Analysis for Current Mode Threshold Logic Gate Designs	**DOMAIN**
VBEP05	Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications	**IEEE 2017-18 VLSI TITLES**
VBEP06	Probability-Driven Multi-bit Flip-Flop Integration With Clock Gating	
VBEP07	A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications	
VBEP08	A 0.1–2-GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS	
VBEP09	Conditional-Boosting Flip-Flop for Near-Threshold Voltage Application	
VBEP10	An All-MOSFET Sub-1-V Voltage Reference With a−51-dB PSR up to 60 MHz	
VBEP11	A 65-nm CMOS Constant Current Source with Reduced PVT Variation	
VBEP12	A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy	
VBEP13	Preweighted Linearized VCO Analog-to-Digital Converter	
VBEP14	A 100-mA, 99.11% Current Efficiency, 2-mVppRipple Digitally Controlled LDO with Active Ripple Suppression	
VBEP15	Sense Amplifier Half-Buffer (SAHB): A Low-Power High-Performance Asynchronous Logic QDI Cell Template	
VBEP16	On Micro-architectural Mechanisms for Cache Wear out Reduction	
VBEP17	Energy-Efficient TCAM Search Engine Design Using Priority-Decision in Memory Technology	
VBEP18	A 92-dB DR, 24.3-mW, 1.25-MHz BW Sigma–Delta Modulator Using Dynamically Biased Op Amp Sharing	
VBEP19	A 0.45 V 147–375 nW ECG Compression Processor With Wavelet Shrinkage and Adaptive Temporal Decimation Architectures	